AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-20 (Cancelled):

Claim 21 (Currently Amended): A wafer prober for probing a semiconductor wafer comprising: ~~having~~

a ceramic substrate; and

a conductor layer formed on a surface of said ceramic substrate, said conductor layer directly contacting a surface of the semiconductor wafer during a probing of the semiconductor wafer, wherein said ceramic substrate comprises at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

Claim 22 (Previously Presented): The wafer prober according to Claim 21, wherein said ceramic substrate is equipped with a temperature control means.

Claim 23 (Previously Presented): The wafer prober according to Claim 22, wherein said temperature control means is a heating element.

Claim 24 (Previously Presented): The wafer prober according to Claim 21, wherein said ceramic substrate is equipped with a Peltier device.

Claim 25 (Previously Presented): The wafer prober according to claim 21, wherein channels are formed on said surface of said ceramic substrate.

Claim 26 (Previously Presented): The wafer prober according to Claim 25, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

Claim 27 (Previously Presented): The wafer prober according to Claim 21, wherein said conductor layer is a chuck top conductor layer.

Claim 28 (Previously Presented): The wafer prober according to Claim 21, wherein said conductor layer has a thickness of 1 to 20 μm.

Claim 29 (Previously Presented): The wafer prober according to Claim 21, wherein a noble metal layer is formed on said surface of said conductor layer.

Claim 30 (Previously Presented): The wafer prober according to Claim 21, wherein said conductor layer comprises nickel.

Claim 31 (Previously Presented): The wafer prober according to Claim 21, wherein said conductor layer comprises a titanium layer, a molybdenum layer and a nickel layer in this order.

Claim 32 (Currently Amended): The wafer prober according to Claim 21, which performs [[a]] the probing of the [[a]] semiconductor wafer by pressing a probe card on the wafer and applying an electric voltage to the semiconductor wafer.

Claim 33 (Currently Amended): A wafer prober for probing a semiconductor wafer ~~having~~ comprising:

a ceramic substrate; and

a conductor layer formed on a surface of said ceramic substrate, wherein the conductor layer is directly contacting a surface of the semiconductor wafer during a probing of the semiconductor wafer, and at least one conductor layer formed inside said ceramic substrate.

Claim 34 (Previously Presented): The wafer prober according to Claim 33, wherein said ceramic substrate is equipped with a temperature control means.

Claim 35 (Previously Presented): The wafer prober according to Claim 34, wherein said temperature control means is a heating element.

Claim 36 (Previously Presented): The wafer prober according to Claim 21, wherein said conductor layer comprises porous material.

Claim 37 (Previously Presented): The wafer prober according to Claim 36, wherein said conductor layer has a thickness of 1 to 200 μm.

Claim 38 (Previously Presented): The wafer prober according to Claim 36, wherein said conductor layer is a chuck top conductor layer.

Claim 39 (Previously Presented): The wafer prober according to Claim 36, wherein said ceramic substrate is equipped with a temperature control means.

Claim 40 (Previously Presented): The wafer prober according to Claim 36, wherein said ceramic substrate is equipped with a Peltier device.

Claim 41 (Previously Presented): The wafer prober according to Claim 39, wherein said temperature control means is a heating element.

Claim 42 (Previously Presented): The wafer prober according to Claim 36, wherein at least one conductor layer is formed inside said ceramic substrate.

Claim 43 (Previously Presented): The wafer prober according to Claim 36, wherein channels are formed on said surface of said ceramic substrate.

Claim 44 (Previously Presented): The wafer prober according to Claim 43, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

Claim 45 (Previously Presented): The wafer prober according to Claim 36, wherein a noble metal layer is formed on the surface of said conductor layer.

Claim 46 (Previously Presented): The wafer prober according to Claim 36, wherein said conductor layer comprises nickel.

Claim 47 (Previously Presented): The wafer prober according to Claim 36, wherein said conductor layer comprises a titanium layer, a molybdenum layer and a nickel layer in this order.

Claim 48 (Currently Amended): A ceramic substrate for a wafer prober for probing a semiconductor wafer which has a conductor layer formed on a surface thereof, wherein the conductor layer directly contacts a surface of the semiconductor wafer during a probing of the semiconductor wafer, wherein said ceramic substrate is composed of at least one selected from the group consisting of nitride ceramics, carbide ceramics and oxide ceramics.

Claim 49 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 48, wherein said ceramic substrate is equipped with a temperature control means.

Claim 50 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 49, wherein said temperature control means is a heating element.

Claim 51 (Previously Presented): The ceramic substrate for a. wafer prober according to Claim 48, wherein said ceramic substrate is equipped with a Peltier device.

Claim 52 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 48, wherein channels are formed on said surface of said ceramic substrate.

Claim 53 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 52, wherein said channels formed on said surface of said ceramic substrate are provided with air suction holes.

Claim 54 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 48, wherein said conductor layer is composed of porous material.

Claim 55 (Currently Amended): A ceramic substrate for a wafer prober which has a conductor layer formed on a surface thereof, wherein the conductor layer directly contacts a surface of a semiconductor wafer during a probing of a semiconductor wafer, and at least one conductor layer formed inside said ceramic substrate.

Claim 56 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 55, wherein said ceramic substrate is equipped with a temperature control means.

Claim 57 (Previously Presented): The ceramic substrate for a wafer prober according to Claim 56, wherein said temperature control means is a heating element.